0.5 μm GaN RF power bar technology space evaluation

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ABSTRACT

This paper describes the test plan and the main results achieved by UMS during a space evaluation of its second generation 0.5 μm GaN RF power bar technology, called GH50-20. The space evaluation tests results are summarised: a life time higher than 5.10^6 h @ 200 °C is found, SEE, TID and DD radiation hardness safe area were defined, and failure rate below 10 FIT @ 200 °C was determined. The results also include demonstration of representative integrated circuits up to 130 W RF power level when operated in L-band in continuous wave (CW) mode. The GH50-20 technology has successfully passed the space evaluation program and is deemed suitable for use in space.

1. Introduction

Many III-V compound semiconductor manufacturers are meanwhile working on GaN technologies. Most of them have started with lower frequencies (RF and microwave) and developed 0.5–0.4 μm AlGaN/GaN processes and corresponding devices. These devices have been offered in flange mount packages since the thermal management of GaN devices are critical and such packages are the best in terms of heat transfer. Some typical examples are shown in Table 1.

The trend to offer GaN devices also for higher frequencies requires the integration of the complete or at least a part of the matching network into the package. This option offers better robustness regarding assembly spreads. As can be seen at almost all GaN device manufacturers, packaged transistors remain, up to C-band, a good and cost effective solution. The impedance matching can be easily made outside of the package on the PCB or the ceramic board. Above C-band internally matched amplifiers are being used, first with external matching circuitry and at higher frequencies (X-band and above) by using a monolithic integration. However, the monolithic integration requires a totally different technology which includes the manufacturing of resistors, transmission lines, MIM capacitors and other circuit elements.

UMS has qualified a second generation of 0.5 μm gate length power bar technology for microwave applications [1], useable up to C-band, called GH50-20. This technology has been optimised from the first generation [2] to improve yield, performance and reliability figures. Enabling a full transfer from the first to the second generation, a space evaluation program was launched on the GH50-20 technology in order to be included in the ESA European Preferred Parts List (EPPL).

2. Technology

GH50-20 technology is based on 4" diameter wafers using AlGaN/GaN/SiC epitaxy. The Ni/Pt/Au 0.5 μm gate is formed using optical stepper lithography.

Two metallization layers can be used for implementing interconnects, high frequency lines and for the source terminated field plate. The second metallization layer also provides air bridges to overcome topologies and cross previous structures with low parasitic capacitance.

The surface treatment and SIN passivation layer stack have been optimised to minimise gate leakage current. Power transistors are designed with an optimised source terminated field plate allowing both high biasing voltage (50 V nominal) and operation up to C band. Sources are grounded using metalized via holes through 100 μm thinned SiC substrate.

3. Test vehicles

The space evaluation tests of the GH50-20 technology were performed on three different test vehicles AuSn soldered in metal ceramic packages. A Dynamic Evaluation Circuit (DEC) consisting of 4 × 400 μm transistor, which is the elementary cell used in the power bar product, was used for highly accelerated life tests. The DECs were matched externally on board using two different matching conditions: a first one corresponding to an operation at PAEmax level, achieving a nominal RF output power of 10 W at 3GHz, and a second one corresponding to a large excursion of the load-cycle characteristics (open-load test board), achieving a nominal RF output power above 6 W at...
3GHz. The comparison between the load-cycles is presented in Fig. 1. These two different characterization boards were used at each interim measurement in order to check any difference in term of reliability behaviour all along the test execution. For RF Life Test only the open-load test board was used. Note that all the DEC characteristics presented in this paper were measured with the PAEmax test board, except for the RFLT data as mentioned previously.

In addition, two Representative Integrated Circuits (RIC), named RIC2 and RIC3 (Fig. 2), with a total transistor gate width of 12 mm and 25.6 mm respectively, were used in order to gain further insights on failure rate and behaviour of bigger transistors. RIC2 and RIC3 were matched externally to achieve a nominal RF output power of 40 W and 130 W at 1.3GHz.

The junction temperature was estimated based on thermal modelling using finite element simulation. Thermal model were validated through thermal measurements like Raman, thermo-reflectance and infra-red spectroscopy [3].

4. Test plan

The test plan is mainly based on the ESA ESCC 2265010 [4] - Evaluation test programme for discrete microwaves semiconductors - as the dedicated technology is to provide discrete transistors. Historically, this standard was conceived for Si and GaAs semiconductor technologies, so an adaptation of the specified tests was necessary to adhere to the GaN technology. Furthermore, the amount of tests, test duration and used devices were significantly increased (see Table 2) in order to generate more data, provide further insight and improve statistical confidence for the space evaluation data set.

Storage tests were performed on two wafers selected from the same process batch lot, in order to assess diffusion mechanisms between different technological layers (e.g. metal layers).

Robustness tests consisted of a High Temperature Reverse Bias (HTRB) test and a RF Step Stress Test (RFSST) performed on DEC devices. The HTRB test was performed in order to assess the robustness of the Schottky gate contact under high electric field operation, while the RFSST aimed to identify the DC and RF electrical limits of the technology allowing the Absolute Maximum Rating (AMR) of the technology to be defined.

Wear-out behaviour was evaluated through two High Temperature Operating Life (HTOL) tests, on DEC devices. The objective here was to identify thermally activated wear-out mechanisms, to evaluate an activation energy and to provide a life time evaluation.

Failure rate was evaluated though DC Life Tests (DCLT) and RF Life Tests (RFLT) performed on DEC, RIC2 and RIC3 devices.

Finally, a thorough radiation test campaign was performed to evaluate the radiation robustness of the GH50-20 technology, including Displacement Damage (DD), Total Ionizing Dose (TID) and Single Event Effect (SEE) tests. All radiation tests have been performed on the largest transistor device (RIC3) with a gate width of 25.6 mm in order to obtain the highest probability of interaction between the radiation particles and the active area of the devices.

5. Space evaluation test results

5.1. Storage test

Two complete wafers were stressed in an oven at ambient air and elevated temperatures at no biasing condition. The PCM structures on the wafers were measured at different time intervals throughout the 2000 h test duration. Wafer 1 was stressed at \( T = 275 \, ^\circ C \) and wafer 2 at \( T = 300 \, ^\circ C \).

The resistance of the Metal_1 layer (R_M1) was the parameter exhibiting the main variation. An activation energy of \( E_a = 2.27 \, eV \) was evaluated, leading to a TTF (at \( 200 \, ^\circ C \)) = \( 6.7 \cdot 10^6 \, h \). This duration is well above the end-of-life target and the diffusion mechanisms are therefore not a risk to the operation of this technology under nominal operation.

5.2. Robustness tests

A High Temperature Reverse Bias (HTRB) test was carried out on 10 DEC devices, at \( V_{DS} = 50 \, V \), \( V_{GS} = -7 \, V \), and \( T_{amb} = 175 \, ^\circ C \). This test has shown no failure after 3000 h test duration, confirming the robustness of the Schottky gate contact under high electric field operation. As an example, the behaviour of the gate leakage current is provided in Fig. 3.

An RF step stress test was carried out on 4 DEC devices at 3 GHz and 50 mA/mm quiescent bias current using the open load test fixture matching conditions. The first voltage step applied was at \( V_{DS} = 50 \, V \).

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**Table 1** Examples of GaN power bar packaged components into metal ceramic flange package.

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part number</th>
<th>Power (W)</th>
<th>Freq (GHz)</th>
<th>VDS (V)</th>
<th>Gain (dB)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMS</td>
<td>CHZ180A-SEB</td>
<td>180</td>
<td>1.2–1.4</td>
<td>45</td>
<td>&gt; 14</td>
<td>52%</td>
</tr>
<tr>
<td>Sumitomo</td>
<td>SGK5867-100A</td>
<td>100</td>
<td>5.85–6.75</td>
<td>24</td>
<td>13</td>
<td>45%</td>
</tr>
<tr>
<td>Wolfspeed</td>
<td>CGHV50200F</td>
<td>180</td>
<td>4.4–5</td>
<td>40</td>
<td>&gt; 12</td>
<td>42%</td>
</tr>
<tr>
<td>Qorvo</td>
<td>TG3929-1RM</td>
<td>100</td>
<td>3.5</td>
<td>28</td>
<td>17.4</td>
<td>45%</td>
</tr>
</tbody>
</table>
The stress was then increased step by step: Initially, the RF input power (PIN) was adjusted to give \( P_{\text{OUT}} \) at the PAE max operating condition. The RF stress was then increased by incrementing the input power by +1 dB and +2 dB. Each step was stressed for a duration of at least 48 h at the incremental value of \( P_{\text{IN}} \). After completion of the RF step stress cycle, \( V_{\text{DS}} \) was increased by +2.5 V and \( P_{\text{IN}} \) was set to the PAE max condition once again to start the RF step stress cycle. The overall procedure was repeated until a failure occurred. The test reached \( V_{\text{DS}} = 80 \) V & \( P_{\text{IN}}@\text{PAEmax} + 1 \) dB when the first two electrical failures occurred. Electrical characterization shows a diode degradation on the two failed devices only at the last step, no preliminary degradation was observed (see Fig. 4). These results were above the level of robustness already evaluated during the UMS internal qualification program, confirming the AMR (Absolute Maximum Ratings) of the GH50-20 technology that was set at \( V_{\text{DS}} = 60 \) V and with an RF compression level value of \( \text{PIN} \) equal to \( \text{PIN}@\text{PAEmax} + 1 \) dB.

### 5.3. Wear-out evaluation

Two HTOL tests (see Table 2) were performed at two different junction temperatures. The test durations when this paper was submitted were 9000 h for HTOL1 (\( T_j = 320 \) °C) and 5000 h for HTOL2 (\( T_j = 340 \) °C). Only one device has reached the power drift failure criteria (drift of -1 dB of the output power at PAEmax) in HTOL1 after 6000 h of test (see Fig. 5). This failure criteria was reached at 6000 h when measured on the open-load test board configuration, while it was reached only after 7000 h when measured with the PAEmax test board. This result suggests that the load-cycle conditions have an impact on the reliability level evaluation.

The failure signature is identical to the ones already observed on GaN technology and can be attributed to inverse piezoelectric effect [5][6]. Based on the use of the activation energy (\( E_a = 1.62 \) eV) evaluated

![Fig. 3. Gate leakage current \( (V_{\text{DS}} = 50 \) V & \( V_{\text{GS}} = -7 \) V) variation during HTRB test on DEC. Interim measurements done at room temperature.](image)

![Fig. 4. Gate leakage current \( (V_{\text{DS}} = 50 \) V & \( V_{\text{GS}} = -7 \) V) variation during RFSST test on DEC. Interim measurements done at room temperature.](image)

![Fig. 5. Saturated output power variation during HTOL test on DEC at two different junction temperatures. Interim measurements done at room temperature.](image)
The failure rate of the GH50-20 technology evaluated during the space evaluation test plan was based upon the life test data from 67 devices that went through the DC and RF aging tests described above, and including the DEC HTOL test results that did not exhibit any catastrophic failures. A total of 207,000 component hours have been accumulated, distributed over HTOL, DC and RF Life Tests. Considering a confidence level of 60%, and a conservative activation energy of 1.5 eV, a failure rate of 9 FIT is evaluated for an operation at Tj = 200 °C, and less than 1 FIT for operation in space environment with a maximum junction temperature of 160 °C (see Table 3).

5.5. Radiation tests

The DD tests performed on 6 units show no influence of proton irradiation on the electrical performance up to a tested fluence of 10^12 p/cm²: the maximum increase of gate-leakage current was only 0.2 μA/mm, and the maximum output power decrease was 0.2 dB, which is in the range of the test bench reproducibility level.

Similarly, the TID tests show no influence of Co60 irradiation up to a final tested cumulated dose of 274 krad. This test was performed on 10 devices, through 2 radiation test sequences with DC interim measurements: a first one up-to a cumulative dose of 94 krad, and the second one up-to a cumulative dose of 274 krad. Three (3) biasing conditions were evaluated, for different couples of VGS & VDS:
- 2 units at VGS = 0 V / VDS = 0 V.
- 3 units at VGS = -7 V / VDS = 50 V (common biasing).
- 5 units at VGS = -7 V / VDS = 80 V (common biasing).

A 168 h annealing period at 100 °C was performed after the radiation step. All the measurements performed during the radiation period, during intermediate characterization steps, and before/after an annealing period at the end of the radiation period did not exhibit any relevant variation of the electrical characteristics of the devices, whatever their biasing conditions during radiation. As an example, the gate leakage current measured at VDS = 40 V is reported in Fig. 8.

Finally, the SEE tests were performed in 3 different operating modes: DC in semi-on-state mode, DC in pinch-off mode, and DC + RF mode. SEE limits have been assessed by mean of multi-runs of Heavy Ion radiation with fluence levels up to 10^10 ions/cm². A gradual increase of the leakage currents was observed for all the different tests. It was noticed that the devices failed when reaching the area of 1 mA for the gate current during real time monitoring. This gate current increase was found to be cumulative and did not recover when the devices were unbiased as can be seen in Figs. 9 and 10. After test, the failure was identified as a burn-out occurring in the gate area of the device. So the degradation mode is based on a cumulative damage that increases with increasing fluence. This implies that SEE test results are depending on fluence targeted level and an appropriate value of fluence for such testing needs to be carefully considered.

In DC semi-on-state mode, a bias level of VDS = 65 V and ID = 50 mA/mm under Xenon (LET = 62.5) @ 10^12 ions/cm² has been validated on three parts.

In DC + RF mode, VG excursions were extrapolated from simulations at different PNF levels and compared to the failure limit observed during the DC + RF tests (Fig. 11). It was observed that:
- Failures occurred at VGS < −6 V under Xenon exposure at a fluence of 10^12 ions/cm².
- No failure was observed up to VGS = −10 V under Rhodium exposure at a fluence of 10^12 ions/cm², and was validated for VGS = −9 V on three different devices.

Looking at the simulation of VDS shown in Fig. 12, it is apparent that there is no correlation with PIN in compression and no failure was observed in the DC + RF tests in such conditions, showing a robustness of at least up to 125 V voltage swings.
In conclusion, SEE results allowed to define a secure area of operation under heavy ions environment:

- The semi-on-state limit under Xenon (LET-Si = 62.5 MeV.mg/cm²) was established at VDS = 65 V and ID = 50 mA/mm;
- The maximum RF voltage excursions in gate and drain are such as described into Table 4.

A follow on SEE radiation test campaign is planned to confirm the results and gather more statistics.

6. Conclusion

A formal space evaluation campaign has been performed on the UMS GH50-20 technology, following the ESA/ESCC specification 2265010 with adaptions due to the GaN material. All tests have been
completed successfully and the GH50-20 process is considered suitable for space applications. An EPPL (European Preferred Parts List) entry application is under submission. Following the successful space evaluation, a capability approval is on-going to further simplify the European access to space rated and qualified hardware by obtaining QPL (Qualified Parts List) listing for a family of hermetic packaged GH50-20 power transistors.

CRediT authorship contribution statement


Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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TID radiation tests have been performed at the ESTEC ESA facility in Netherlands.

SEE and DD radiation tests have been performed in collaboration with TRAD at the UCL facility in Belgium.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.microrel.2020.113894.

References


Table 4

Maximum RF voltage excursion in gate and drain.

<table>
<thead>
<tr>
<th>LET (Si) (MeV.mg/cm²)</th>
<th>$V_{GS}$ max (V)</th>
<th>$V_{DS}$ max (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xe – 62.5</td>
<td>−6</td>
<td>125</td>
</tr>
<tr>
<td>Rh – 46.1</td>
<td>−9</td>
<td>125</td>
</tr>
</tbody>
</table>

![Fig. 12. $V_{DS}$ excursion in DC + RF mode at different PIN levels.](image-url)